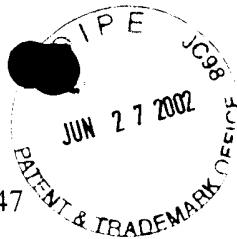


Docket No.: 50090-247



**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Osamu HASHIMOTO, et al.

Serial No.: 09/730,750

Group Art Unit: 2856

Filed: December 07, 2000

Examiner: Jimmy Nguyen

For: APPARATUS AND METHOD OF INSPECTING SEMICONDUCTOR  
INTEGRATED CIRCUIT

**AMENDMENT**

Commissioner for Patents  
Washington, DC 20231

Sir:

The following amendments and remarks are respectfully submitted in response to  
the Office Action dated January 30, 2002.

**IN THE SPECIFICATION:**

Please replace the paragraph beginning at page 11, line 17, with the following  
rewritten paragraph:

--Further, in the structure of the burn-in board 12 according to the present  
embodiment, a space is ensured between the burn-in board 12 and the exchange board 22 by  
means of the spacers 20. Providing a bypass capacitor on a power line pattern or a GND  
pattern is effective for eliminating noise which would otherwise be superimposed on the  
power line pattern or the GND pattern. According to the present embodiment, a bypass  
capacitor can be placed in the space defined between the burn-in board 12 and the exchange  
board 22. In this respect, the structure of the burn-in board 12 according to the present

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JUN 27 2002  
PATENT & TRADEMARK OFFICE  
WASHINGTON, DC 20231